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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,602	BRINK ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The claim 1 recites the subject matter "the interrupt information" in lines 5-6. However, it has not been specifically clarified in the claim 1. Therefore, the Examiner presumes that the term "the interrupt information" could be considered as --an interrupt information-- in light of the specification since it is not defined in the claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13-16, 18-22, and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Athenes et al. [US 6,192,441 B1; hereinafter Athenes].

Referring to claim 13, Athenes discloses a method (i.e., method of postponing processing of interrupts by a microprocessor; See Abstract) comprising:

- receiving an interrupt request (i.e., event justifying an interruption) at an interrupt controller (i.e., interrupt control device 3 of Fig. 1; See col. 3, lines 19-22);
- acquiring, at the interrupt controller (i.e., at said interrupt control device), interrupt information corresponding to the interrupt request (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44); and
- passing the interrupt information from the interrupt controller (i.e., said interrupt control device) to a memory device (i.e., RAM 2 of Fig. 1) without passing the interrupt information to a processor (i.e., microprocessor 1 of Fig. 1; See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of

the preceding event, and further said logic circuit behaves as a DMA controller inherently anticipates passing the interrupt information from the interrupt controller to a memory device without passing the interrupt information to a processor).

Referring to claim 14, Athenes teaches

- polling the memory device (i.e., RAM 2 of Fig. 1) to check for the interrupt information (See col. 5, lines 61-63).

Referring to claim 15. Athenes teaches

- polling is performed by the processor (i.e., microprocessor 1 of Fig. 1) at a time independent from a time the interrupt request (i.e., event justifying an interruption) is received by the interrupt controller (i.e., interrupt control device 3 of Fig. 1; See col. 2, lines 59-67).

Referring to claim 16. Athenes teaches

- performing an interrupt function (i.e., interrupt processing) based on the interrupt information (See col. 5, line 61 through col. 6, line 11).

Referring to claim 18, Athenes teaches

- the memory device (i.e., RAM 2 of Fig. 1) and the interrupt controller (i.e., interrupt control device 3 of Fig. 1) are located in separate chips (See col. 3, lines 9-15; i.e., wherein in fact that RAM is common to the different elements of the system, and is connected to the logic circuit of interrupt control device inherently anticipates that the memory device and the interrupt controller are located in separate chips, e.g., RAM memory chip and logic circuit chip).

Referring to claim 19. Athenes teaches

- passing the interrupt information (i.e., the origin of interrupt and reason for the interruption event) from the interrupt controller (i.e., interrupt control device 3 of Fig. 1) to the memory device (i.e., RAM 2 of Fig. 1; See col. 3, lines 19-25) includes writing the interrupt information to the memory device at a memory location according to configuration information (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67).

Referring to claim 20. Athenes teaches

- the configuration information (i.e., address of Word for interrupt in RAM 2 in Fig. 1) is stored in the interrupt controller (i.e., said address is stored in registers 6,7 of said interrupt control device 3 in Fig. 1).

Referring to claim 21. Athenes discloses a method (i.e., method of postponing processing of interrupts by a microprocessor; See Abstract) comprising:

- receiving an interrupt request (i.e., event justifying an interruption) at a chipset[cf.] (i.e., interrupt control device 3 of Fig. 1), the chipset (i.e., said interrupt control device) connecting to a processor (i.e., microprocessor 1 of Fig. 1; See col. 3, lines 9-22);
- acquiring, at the chipset (i.e., at said interrupt control device), interrupt information corresponding to the interrupt request (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44); and
- storing the interrupt information at a memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67) without notifying the processor (i.e., said microprocessor) the interrupt request (See col. 2, lines 59-67 and col. 3, lines

[cf.] chipset - a number of integrated circuits designed to perform one or more related functions, e.g., FIFO, registers, logic circuit in the interrupt control device for interrupt controlling function

27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller inherently anticipates storing the interrupt information at a memory location without notifying the processor the interrupt request); and

- polling the memory device (i.e., RAM 2 of Fig. 1) to check for the interrupt information (See col. 5, lines 61-63), wherein
    - polling is performed at a time independent from a time the interrupt request (i.e., event justifying an interruption) is received at the chipset (i.e., said interrupt control device; See col. 2, lines 59-67).

Referring to claim 22, Athenes teaches

- polling is performed by the processor (i.e., microprocessor 1 of Fig. 1; See col. 5, lines 61-63).

Referring to claim 24, Athenes teaches

- performing an interrupt function (i.e., interrupt processing) based on the interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22) stored in the memory location (See col. 5, line 61 through col. 6, line 11).

Referring to claim 25, Athenes teaches

- storing the interrupt information at the memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67) includes storing the interrupt information (i.e., the origin of interrupt and reason for the interruption event) in a memory device (i.e., RAM 2 of Fig. 1) separate from the processor (i.e., microprocessor 1 of Fig. 1) and the chipset (i.e., interrupt control device 3 of Fig. 1; See col. 3, lines 9-15; i.e., wherein in

fact that RAM is common to microprocessor and to the different elements of the system, and is connected to the logic circuit of interrupt control device inherently anticipates a memory device separate from the processor and the chipset).

Referring to claim 26, Athenes teaches

- storing the interrupt information at the memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67) includes storing the interrupt information (i.e., the origin of interrupt and reason for the interruption event) at the memory location according to a configuration information (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67).

Referring to claim 27, Athenes teaches

- the configuration information (i.e., address of Word for interrupt in RAM 2 in Fig. 1) is stored in the chipset (i.e., said address is stored in registers 6,7 of said interrupt control device 3 in Fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of

each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh [US 5,935,233 A] in view of Athenes [US 6,192,441 B1].

Referring to claim 1, Jeddeloh discloses an integrated circuit (i.e., PCI host bridge 56 of Fig. 2) comprising:

- a peripheral interface (i.e., first PCI interface 86 of Fig. 2);
- a memory interface (i.e., memory interface 84 of Fig. 2) to communicate with a memory device (i.e., system memory 58 of Fig. 2; See col. 3, lines 54-56);
- a processor interface (i.e., processor interface 82 of Fig. 2) to communicate with a processor (i.e., processor 52 of Fig. 2; See col. 3, lines 51-53); and
- a logic circuit (i.e., control switch 90 of Fig. 2) connected to the peripheral interface (i.e., said first PCI interface is connected to said Control switch in Fig. 2), wherein
    - the logic circuit (i.e., said control switch) is also connected to the processor interface and the memory interface (i.e., said first PCI interface and said processor interface are connected to said control switch in Fig. 2).

Jeddeloh does not teach the peripheral interface receives an interrupt request; and the logic circuit acquires an interrupt information associated with the interrupt request, wherein the logic circuit is to pass the interrupt information to the memory device without passing the interrupt information to the processor interface.

Athenes discloses an apparatus for postponing processing of interrupts by a microprocessor (See Abstract), wherein

- a peripheral interface (i.e., 16-bits buses between entities U1-U3 and interrupt control device 3 in Fig. 1) receives an interrupt request (i.e., event justifying an interruption; See col. 3, lines 19-22); and
- a logic circuit (i.e., interrupt control device 3 of Fig. 1) acquires an interrupt information (i.e., the origin of interrupt and reason for the interruption event) associated with the interrupt request (See col. 3, lines 21-22 and col. 4, lines 38-44), wherein
    - the logic circuit (i.e., said interrupt control device) is to pass the interrupt information to a memory device (i.e., RAM 2 of Fig. 1) without passing the interrupt information to a processor interface (See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller implies that the logic circuit passes the interrupt information to a memory device without passing the interrupt information to a processor interface).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said integrated circuit (i.e., interrupt control device), as disclosed by Athenes, in said logic circuit (i.e., control switch), as disclosed by Jeddeloh, for the advantage of avoiding a risk of operation error that a subsequent interrupt signal (i.e., event) interrupts the processing of a preceding interrupt of the same type, issued by a same entity (See Athenes, col. 2, line 67 through col. 3, line 3).

Referring to claim 2, Athenes teaches

- a memory unit (i.e., FIFOs 8-10 in Fig. 1) to store the interrupt information (i.e., the origin of interrupt and reason for the interruption event) before the interrupt information is passed to the memory interface (i.e., n-bits bus 5 between logic circuit 4 and RAM 2 in Fig. 1; See col. 5, lines

32-48).

Referring to claim 3, Athenes teaches

- a configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1) to store configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-52) indicating a location in the memory device (i.e., RAM 2 of Fig. 1) to store the interrupt information (See col. 4, lines 53-67).

Referring to claim 5, Jeddeloh teaches

- a graphics interface (i.e., second PCI interface 88 of Fig. 2) to communicate with a graphics card (i.e., graphics controller 74 of Fig. 2; See col. 3, lines 40-44 and 62-67).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh [US 5,935,233 A] in view of Athenes [US 6,192,441 B1] as applied to claims 1-3 and 5 above, and further in view of Tseng et al. [US 6,816,918 B2; hereinafter Tseng].

Referring to claim 4, Jeddeloh, as modified by Athenes, discloses all the limitations of the claim 4, including the configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1; Athenes) having a memory device (i.e., registers 6 and 7 in Fig. 2; Athenes) to store the configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See Athenes, col. 3, lines 30-35 and col. 4, lines 45-52), except that does not expressly teach that said memory device is a read only memory device.

Tseng discloses a flexible apparatus for setting configurations using an EEPROM (See Abstract), wherein

- a configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM in Fig. 3) including a read only memory device (i.e., said EEPROM in

Fig. 3) to store a configuration address (i.e., storing address index and its contents; See col. 3, lines 35-39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM), as disclosed by Tseng, in said configuration circuit (i.e., logic circuit and registers), as disclosed by Jeddeloh, for the advantage of providing a method for flexibly configuring default location in the memory device (i.e., default value) of said integrated circuit (i.e., network device) through said read only memory (i.e., EEPROM interface; See Tseng, col. 2, lines 28-30).

8. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al. [US 6,466,226 B1; hereinafter Watson] in view of Athenes [US 6,192,441 B1].

Referring to claim 6. Watson discloses a system (i.e., computer system in Fig. 2) comprising:

- a processor (i.e., one of the one or more processors 110 of Fig. 2; See col. 3, lines 60-64);
- a memory device (i.e., system memory 130 of Fig. 2); and
- a chipset (i.e., chipset 200 of Fig. 2) connected to the processor and the memory device (i.e., said processor and said system memory are connected to said chipset in Fig. 2; See col. 5, lines 19-32).

Watson does not teach the chipset is configured to receive interrupt information and to pass the interrupt information to the memory device without notifying the processor the presence of the interrupt information.

Athenes discloses an apparatus for postponing processing of interrupts by a microprocessor (See Abstract), wherein a chipset (i.e., interrupt control device 3 of Fig. 1) is configured

- to receive interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44) and

- to pass the interrupt information to a memory device (i.e., RAM 2 of Fig. 1) without notifying a processor the presence of the interrupt information (See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller implies that the chipset is configured to pass the interrupt information to a memory device without notifying a processor the presence of the interrupt information).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said chipset (i.e., interrupt control device), as disclosed by Athenes, in said chipset, as disclosed by Watson, for the advantage of avoiding a risk of operation error that a subsequent interrupt signal (i.e., event) interrupts the processing of a preceding interrupt of the same type, issued by a same entity (See Athenes, col. 2, line 67 through col. 3, line 3).

Referring to claim 7, Watson teaches

- the chipset (i.e., chipset 200 of Fig. 2) includes a graphic and memory control hub (i.e., GMCH 210 of Fig. 2) to process graphic and memory information (See col. 5,lines 19-23) and to provide access between the processor (i.e., said one of the one or more processors 110 of Fig. 2) and the memory device (i.e., system memory 130 of Fig. 2; See col. 5,lines 23-32).

Referring to claim 8, Watson teaches

- the chipset (i.e., chipset 200 of Fig. 2) includes an input output control hub (i.e., ICH 220 of Fig. 2) connected to the graphic and memory control hub (i.e., GMCH 210 of Fig. 2; See col. 5, lines 28-32) to process input output information between the chipset and external devices (e.g., display 150, USB devices, and AC'97 devices, etc. in Fig. 2; See col. 5, line 32 through col. 6, line 12).

Referring to claim 9, Athenes teaches

- the chipset (i.e., interrupt control device 3 of Fig. 1) includes an interrupt controller (i.e., logic circuit 4 of Fig. 1) to receive the interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44).

Referring to claim 10, Watson, as modified by Athenes, teaches

- the processor (i.e., said one of the one or more processors 110 of Fig. 2 in Watson, which is mapped to microprocessor 1 of Fig. 1 in Athenes) is configured to poll the memory device (i.e., RAM 2 of Fig. 1; Athenes) to check for the interrupt information (See Athenes, col. 5, lines 61-63) at a time independent from a time the interrupt information is received by the chipset (See Athenes, col. 2, lines 59-67).

Referring to claim 11, Watson teaches

- a second processor (i.e., the other one of the one or more processors 110 of Fig. 2; See Watson, col. 3, lines 60-64) connected to the chipset (i.e., chipset 200 of Fig. 2).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson [US 6,466,226 B1] in view of Athenes [US 6,192,441 B1] as applied to claims 6-11 above, and further in view of what was well known in the art, as exemplified by Callway et al. [US 6,279,067 B1; hereinafter Callway].

Referring to claim 12, Watson, as modified by Athenes, discloses all the limitations of the claim 12, including the processor (i.e., said one of the one or more processors 110 of Fig. 2 in Watson, which is mapped to microprocessor 1 of Fig. 1 in Athenes) configured to poll the memory device (i.e., RAM 2 of Fig. 1; Athenes) to check for the interrupt information (See Athenes, col. 5, lines 61-65) at a time

independent from a time the interrupt information is received by the chipset (See Athenes, col. 2, lines 59-67), except that does not teach that the second processor is configured to perform said polling.

The Examiner takes Official Notice that the second processor is configured to perform said polling instead of the processor, what was well known to one of ordinary skill in the art, as evidenced by Callway, such that Callway discloses an apparatus for detecting interrupt requests in video graphics and other system (See Abstract), wherein

- a processor (i.e., video graphics processing block 16 of Fig. 2);
- a second processor (i.e., polling block 12 of Fig. 2) is configured to poll a memory device (i.e.,. registers 34, 44 in Fig. 2) to check for an interrupt information (i.e., IRQ flags; See col. 3, lines 22-28 and 51-57) at a time independent from a time the interrupt information is received by the chipset (i.e., VIP slaves 30, 40 in Fig. 2; See col. 3, lines 57-64, i.e., wherein in fact that polling block generates the required signals to access the registers of the VIP slaves, then determines that an interrupt request is pending implies that a second processor is configured to poll a memory device to check for an interrupt information at a time independent from a time the interrupt information is received by the chipset).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have configured said second processor (i.e., the other one of the one or more processors), as disclosed by Watson, for performing said polling, as disclosed by Athenes, for the advantage of the performance of said processor (i.e., video graphics processing block) is not degraded by having to perform said polling functions by implementing said second processor (i.e., polling block) as separate circuitry from said processor (i.e., video graphics processing block; See Callway, col. 3, line 66 through col. 4, line 8).

10. Claims 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athenes [US 6,192,441 B1] as applied to claims 13-16, 18-22, and 24-27 above, and further in view of Callway [US 6,279,067 B1].

Referring to claims 17 and 23, Athenes discloses all the limitations of the claims 17 and 23, respectively, including that polling is performed by the processor (i.e., microprocessor 1 of Fig. 1) a time independent from a time the interrupt request is received by the interrupt controller, which is the chipset (See col. 2, lines 59-67 and col. 5, lines 61-65), except that does not teach that a second processor is configured to perform said polling.

Callway discloses a method for detecting interrupt requests in video graphics and other system (See Abstract), wherein

- a processor (i.e., video graphics processing block 16 of Fig. 2);
- polling is performed by a second processor (i.e., polling block 12 of Fig. 2) a time independent from a time the interrupt information is received by an interrupt controller (i.e., VIP slaves 30, 40 in Fig. 2; See col. 3, lines 57-64, i.e., wherein in fact that polling block generates the required signals to access the registers of the VIP slaves, then determines that an interrupt request is pending implies that polling is performed by a second processor a time independent from a time the interrupt information is received by the interrupt controller).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included polling by said second processor (i.e., polling block), as disclosed by Callway, in said method for performing said polling, as disclosed by Athenes, for the advantage of the performance of said processor (i.e., video graphics processing block) is not degraded by having to perform said polling functions by implementing said second processor (i.e., polling block) as separate circuitry from said processor (i.e., video graphics processing block; See Callway, col. 3, line 66 through col. 4, line 8).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ota [US 2005/0060462 A1] discloses method and system for efficiently directing interrupts.

Davis et al. [US 5,857,090 A] disclose input/output subsystem having an integrated advanced programmable interrupt controller for use in a personal computer.

Williams [US 4,953,072] discloses node for servicing interrupt request messages on a pended bus.

Bronson et al. [US 6,442,634 B2] disclose system and method for interrupt command queuing and ordering.

Sugahara et al. [US 6,684,281 B1] disclose fast delivery of interrupt message over network.

Qureshi et al. [US 5,905,898 A] disclose apparatus and method for storing interrupt source information in an interrupt controller based upon interrupt priority.

Marr et al. [US 6,775,730 B2] disclose system and method for implementing a flexible interrupt mechanism.

Morrison et al. [US 6,470,408 B1] disclose apparatus and method for delivering interrupts via an APIC bus to IA-32 processors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/